AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of the Claims:

1. (currently amended) A memory card having a plurality of non-volatile memories and a memory controller for controlling operation of said plurality of non-volatile memories, wherein

said memory controller performs an access control of said plurality of non-volatile memories in response to an external access instruction, and an alternation control for substituting a storage area of an access error-related non-volatile memory with another storage area;

each of said plurality of non-volatile memories includes management information used for performing said alternation control thereon, said alternation control being performed individually for each of said plurality of non-volatile memories; and

said memory controller causes said plurality of non-volatile memories to operate for parallel access in said access control,

wherein said memory controller controls access to a first address of a first non-volatile memory and said first address

of a second non-volatile memory, when both of said first address of said first non-volatile memory and said first address of said second non-volatile memory are valid, and

wherein said memory controller controls access to a second address of said first non-volatile memory and a third address of said second non-volatile memory, when said second address of said second non-volatile memory is invalid.

2. (currently amended) A memory card having first and second non-volatile memories and a main controller for controlling operation of said first and second non-volatile memories, wherein

said memory controller allocates said first and second non-volatile memories to storage areas of even and odd data of sector data, respectively;

each of said first and second non-volatile memories has management information used for performing an alternation control thereon, said alternation control being performed individually for each of said first and second non-volatile memories;

said memory controller causes said first and second non-volatile memories to operate for parallel access in an access control of said first and second non-volatile memories in response to an external access instruction; and

said memory controller substitutes a storage area of the access error-related non-volatile memory with another storage area in said alternation control of said first and second non-volatile memories,

wherein said memory controller controls access to a first address of said first non-volatile memory and said first address of said second non-volatile memory, when both of said first address of said first non-volatile memory and said second address of said second non-volatile memory do not include an error memory cell, and

wherein said memory controller controls access to a second address of said first non-volatile memory and a third address of said second non-volatile memory, when said third address of said second non-volatile memory includes an error memory cell.

3. (original) A memory card as defined in Claim 1, further comprising buses for connecting respective non-volatile memories to said memory controller so that said respective non-volatile memories are separately access-controlled.

4. (previously presented) A memory card as defined in Claim 1, wherein:

said memory controller includes an ECC circuit for adding an error detection code to write-data written into said

plurality of non-volatile memories to conduct an error detection and correction for read-data from said plurality of non-volatile memories; and

said ECC circuit conducts an input/output operation at an operation frequency which is equal to an input/output operation frequency of said parallel access operated non-volatile memories multiplied by a number of the parallel access operations.

5. (previously presented) A memory card as defined in Claim 1, wherein:

said memory controller includes one or more ECC circuits which add an error detection code to write-data written into said plurality of non-volatile memories and conduct an error detection and correction for read-data from said plurality of non-volatile memories, said one or more ECC circuits being as many as the number of the parallel access operations; and

said one or more ECC circuits perform input/output operations in a parallel manner at an operation frequency which is equal to the input/output operation frequency of said parallel access operated non-volatile memories.

Claims 6-7 (cancelled).

8. (currently amended) A memory controller comprising:

a host interface circuit capable of being input/output operated in accordance with a predetermined protocol;

a memory interface circuit capable of be connected to a plurality of non-volatile memories in parallel; and

a control circuit connected to said host interface circuit and said memory interface circuit,

wherein said control circuit fetches a plurality of management information from said plurality of non-volatile memories, respectively, performs an external interface control via said host interface circuit, an access control of said non-volatile memories via said memory interface circuit responsive to an external access instruction, and an alternation control for substituting a storage area of an access error-related non-volatile memory with another storage area, and causes said plurality of non-volatile memories to parallel access operate in said access control,

wherein said control circuit is capable of accessing a first address of a first non-volatile memory and said first address of a second non-volatile memory in parallel, when both of said first address of said first non-volatile memory and said first address of said second non-volatile memory are valid, and

wherein said control circuit is capable of accessing a second address of said first non-volatile memory and a third

address of said second non-volatile memory in parallel, when said second address of said second non-volatile memory is invalid.

9. (currently amended) A memory controller comprising:

a host interface circuit capable of being input/output operated in accordance with a predetermined protocol;

a memory interface circuit capable of being connected to first and second non-volatile memories in parallel; and

a control circuit connected to said host interface circuit and said memory interface circuit,

wherein said memory controller allocates said first and second non-volatile memories to storage areas of even and odd data of sector data, respectively, fetches first and second management information from said first and second non-volatile memories, respectively, and uses said first and second management information in an alternation control of said first and second non-volatile memories, respectively, causes said first and second non-volatile memories to parallel access operate in an access control of said non-volatile memories in response to an external access instruction, and substitutes storage areas for storage areas in the non-volatile memory in which an access error occurs in the alternation control of said first and second non-volatile memories,

wherein said memory controller is capable of accessing a first address of said first non-volatile memory and said first address of said second non-volatile memory in parallel, when both of said first address of said first non-volatile memory and said first address of said second non-volatile memory do not include an error memory cell, and

wherein said memory controller is capable of accessing a second address of said first non-volatile memory and a third address of said second non-volatile memory in parallel, when said third address of said second non-volatile memory includes an error memory cell.

10. (previously presented) A memory controller as defined in Claim 8, further comprising:

an ECC circuit for adding an error detection code to write-data written into said plurality of non-volatile memories to perform an error detection and correction for read-data from said plurality of non-volatile memories,

wherein said ECC circuit performs an input/output operation at an operation frequency which is equal to an input/output operation frequency of said parallel access operated non-volatile memories multiplied by a number of the parallel access operations.

11. (previously presented) A memory controller as defined in Claim 9, further comprising:

an ECC circuit for adding an error detection code to write-data written into said first and second non-volatile memories to perform an error detection and correction for read-data from said first and second non-volatile memories,

wherein said ECC circuit performs an input/output operation at an operation frequency which is equal to an input/output operation frequency of said parallel access operated non-volatile memories multiplied by a number of the parallel access operations.

12. (original) A memory controller as defined in Claim 8, wherein said memory controller is formed on one semiconductor chip.

13. (currently amended) A memory card comprising:

a control circuit;

a plurality of non-volatile memories;

an external interface circuit connected to an external device; and

a bus, wherein

each of said plurality of non-volatile memories has management information used for performing an address substituting process thereon, said address substituting process being performed individually for each of said plurality of non-volatile memories;

said plurality of non-volatile memories have a plurality of input/output terminals;

said bus has a first bit width, is divided into each of bits having a predetermined number, and is connected to the input/output terminal of a corresponding one of said plurality of non-volatile memories; and

said control circuit performs an access control to said plurality of non-volatile memories, and performs said address substituting process on each of said plurality of non-volatile memories when an access error occurs,

wherein said control circuit is adapted to access a first address of a first non-volatile memory and said first address of a second non-volatile memory in parallel, when both of said first address of said first non-volatile memory and said first address of said second non-volatile memory do not include an error memory cell, and

wherein said control circuit is adapted to access a second address of said first non-volatile memory and a third address of said second non-volatile memory in parallel, when a second address of said third non-volatile memory includes an error memory cell.

Claims 14-15 (cancelled).